NI Digital Electronics FPGA Board

User Manual

Circuit Development Platform

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NATIONAL INSTRUMENTS™

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Conventions

The following conventions are used in this manual:

<>	Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, AO <3..0>.
»	The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.
	This icon denotes a tip, which alerts you to advisory information.
	This icon denotes a note, which alerts you to important information.
	This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on a product, refer to the *Safety Information* and *ESD Warning* sections of Chapter 1, *Overview and Setup*, for information about precautions to take.
bold	Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.
italic	Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.
`monospace`	Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.
`monospace bold`	Bold text in this font denotes the messages and responses that the computer automatically prints to the screen. This font also emphasizes lines of code that are different from the other examples.
Platform	Text in this font denotes a specific platform and indicates that the text following it applies only to that platform.

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1

Overview and Setup

The NI Digital Electronics FPGA Board is a circuit development platform based on the XC3S500E Xilinx Spartan-3E FPGA. Besides the FPGA, the board contains slide switches, LEDs, a two digit seven-segment display, push-buttons, a rotary push-button knob and LEDs for one external clock, Digilent Pmod terminals for external attachments, USB download interface, and large breadboard area for digital electronics circuitry experimentation.

Safety Information

The following section contains important safety information that you must follow when installing and using the hardware.

Do not operate the hardware in a manner not specified in this document and in the user documentation. Misuse of the hardware can result in a hazard. You can compromise the safety protection if the hardware is damaged in any way. If the hardware is damaged, return it to National Instruments for repair.

Clean the hardware with a soft, nonmetallic brush. Make sure that the hardware is completely dry and free from contaminants before returning it to service.

Do not substitute parts or modify the hardware except as described in this document. Use the hardware only with the chassis, modules, accessories, and cables specified in the installation instructions or specifications. You must have all covers and filler panels installed during operation of the hardware.

Do not operate the hardware in an explosive atmosphere or where there may be flammable gases or fumes unless the hardware is UL (U.S.) or Ex (EU) Certified and marked for hazardous locations. The hardware must be in a suitably rated IP 54 minimum enclosure for hazardous locations. Refer to the hardware's user documentation for more information.

You must insulate signal connections for the maximum voltage for which the hardware is rated. Do not exceed the maximum ratings for the hardware.

Do not install wiring while the hardware is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Avoid contact between your body and the connector block signal when hot swapping hardware. Remove power from signal lines before connecting them to or disconnecting them from the hardware.

Operate the hardware only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees:

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence. Typical level for sealed components or coated PCBs.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected. Typical level for most products.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

Operate the hardware at or below the measurement category[1] marked on the hardware label. Measurement circuits are subjected to working voltages[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Measurement categories establish standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of measurement categories:

- Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS[3] voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special hardware, limited-energy parts of hardware, circuits powered by regulated low-voltage sources, and electronics.
- Measurement Category II is for measurements performed on circuits directly connected to the electrical distribution system (MAINS[3]). This category refers to local-level electrical distribution, such as that

[1] Measurement categories, also referred to as overvoltage or installation categories, are defined in electrical safety standard IEC 61010-1 and IEC 60664-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers hardware. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

provided by a standard wall outlet (for example, 115 AC voltage for U.S. or 230 AC voltage for Europe). Examples of Measurement Category II are measurements performed on household appliances, portable tools, and similar hardware.

- Measurement Category III is for measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired hardware such as hardware in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus bars, junction boxes, switches, socket outlets in the fixed installation, and stationary motors with permanent connections to fixed installations.
- Measurement Category IV is for measurements performed at the primary electrical supply installation typically outside buildings. Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

To obtain the safety certification(s) for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

ESD Warning

Caution Although this product has been designed to be as robust as possible, ESD (Electrostatic Discharge) can damage or upset this product. This product must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.

The NI Digital Electronics FPGA Board is designed and intended for use as a development platform for hardware or software in an educational/professional laboratory environment. To facilitate usage, the board is manufactured with its components and connecting traces openly exposed to the operator and the environment. As a result, ESD sensitive (ESDS) components on the board, such as the semiconductor integrated circuits, can be damaged when exposed to an ESD event. To indicate the ESD sensitivity of the NI Digital Electronics FPGA Board, it carries the symbol shown at left.

Unpacking, Transporting, and Storage

When unpacking the NI Digital Electronics FPGA Board from its shipping carton, do not remove the board from the antistatic packaging material until you are ready to complete the installation. Before unwrapping the antistatic packaging, discharge yourself by touching a grounded bare metal surface, touching an approved anti-static mat, or wearing an ESD strap.

When transporting or storing the NI Digital Electronics FPGA Board, first place it in an antistatic container or packaging.

Handling and Setup

Handling the NI Digital Electronics FPGA Board can damage the board components if ESD prevention measures are not applied. Before handling or setup, equalize your potential with the board by touching one of the integrated ESD discharge pads. During all handling and setup, ESD prevention measures must be applied. In addition, the NI Digital Electronics FPGA Board should be handled by the edges. Touching exposed circuits, components or connectors could result in an ESD event.

When setting up the NI Digital Electronics FPGA Board, observe the following guidelines to minimize the potential impact of ESD:

- Assemble desired custom circuitry in the breadboard area.
- Set switches and other controls to initial settings.
- If desired, connect the NI Digital Electronics FPGA Board to a computer by using the USB port.
- Plug the power adapter into the +15 VDC power supply port.
- Plug the AC/DC power supply brick into an appropriate AC outlet.
- Move the board power switch ON.

Operation

When operating the NI Digital Electronics FPGA Board, ESD can cause upset as well as damage to the board components. Therefore, apply ESD prevention measures whenever operating the NI Digital Electronics FPGA Board. In addition, observe the following guidelines:

- Do not manipulate or change the circuitry the breadboard area while the board is powered on.
- Do not touch exposed traces or components on the board while the board is powered on.
- Exercise caution when manipulating switches, buttons, knobs, and other controls while the board is powered on.

ESD Prevention Measures

ESD prevention measures focus on reducing or eliminating the build-up of static charge that may result in an ESD event that could damage or upset sensitive electronics. To minimize the potential for an ESD event, implement the following measures:

- Perform all work at an approved work station.
- Use an approved antistatic mat to cover your work surface.
- Wear a conductive wrist strap attached to the antistatic mat and a good earth ground.
- Before handling or beginning work, equalize your potential with the board by touching one of the ESD discharge pads.

Installation and Setup

This section describes what you need to get started with the NI Digital Electronics FPGA Board and how to install your software and set up your board.

What You Need to Get Started

The following items are necessary to set up and use the NI Digital Electronics FPGA Board:

- ❑ The NI Digital Electronics FPGA Board kit containing the following:
  - The NI Digital Electronics FPGA Board
  - Standard USB type A-to-mini B cable
  - +15 VDC, 650 mA power adapter
  - *NI Digital Electronics FPGA Board Driver* CD, which contains the NI Digital Electronics FPGA Board driver, readme, and user documentation

- ❑ One of the following software packages:
  - NI LabVIEW, version 8.6 or later, and the LabVIEW FPGA Module, version 8.6 or later, and the following:
    - PC running Windows Vista or Windows XP Pro x32 Service Pack 1 or 2
    - The *LabVIEW Release Notes* and the *LabVIEW FPGA Module Release Notes*

    or
  - Xilinx iMPACT software, version 10.*x* or later, part of the ISE WebPACK software kit, available from `www.xilinx.com/ise`, and the following:
    - PC running Windows Vista/XP
    - The *ISE Design Suite Release Notes and Installation Guide*
- ❑ (Optional) NI ELVIS II Series Benchtop Workstation, AC-DC power supply, high-speed USB 2.0 cable, NI ELVISmx 4.0 or later software CD, and the *Where to Start with NI ELVIS II Series* document

Installation and Setup Instructions

To install and set up the NI Digital Electronics FPGA Board, complete the following steps.

1. Install the software you are going to use.
   a. Install NI LabVIEW as described in the *LabVIEW Release Notes*.
   b. Install the LabVIEW FPGA Module as described in the *LabVIEW FPGA Module Release Notes*.
   c. Install the NI Digital Electronics FPGA Board driver as described in *NI Digital Electronics FPGA Board Driver Readme*.
   d. (Optional) Install the NI ELVISmx software as described in the installation instructions on the software CD.

   or

   a. Install the Xilinx ISE software kit as described in the *ISE Design Suite Release Notes and Installation Guide*.
   b. Install the NI Digital Electronics FPGA Board driver as described in *NI Digital Electronics FPGA Board Driver Readme*.
2. Restart the PC if prompted.

3. Connect the NI Digital Electronics FPGA Board as described in one of the following sections:
   - **Stand-Alone Mode**—To connect the NI Digital Electronics FPGA Board in stand-alone mode connected only to a PC, go to the *Stand-Alone Mode* section.
   - **NI ELVIS Mode**—To connect the NI Digital Electronics FPGA Board in NI ELVIS mode, as an NI ELVIS prototyping board, go to the *NI ELVIS Mode* section.

Stand-Alone Mode

The NI Digital Electronics FPGA Board can be used on a desktop as a stand-alone—or self-contained—device in stand-alone mode. The board requires a PC for new program download and optional application control/monitoring purposes. To install and set up the NI Digital Electronics FPGA Board in stand-alone mode, complete the following steps.

1. Connect the USB type A connector to the USB connector on the host PC.
2. Connect the USB type mini B connector to the NI Digital Electronics FPGA Board USB connector.
3. Connect the +15 VDC power adapter to the power connector on the NI Digital Electronics FPGA Board, then plug the power supply into a wall outlet.
4. Power on the NI Digital Electronics FPGA Board by moving the power switch to the ON position.

   (Windows XP) Windows recognizes any newly installed device the first time the computer reboots after hardware is installed. On some Windows systems, the Found New Hardware Wizard opens with a dialog box for every NI device installed. **Install the software automatically (Recommended)** is selected by default. Click **Next** or **Yes** to install the software for the device and the USB cable ports.

   The green LD-G LED lights, indicating a good connection.

NI ELVIS Mode

In NI ELVIS mode, the NI Digital Electronics FPGA Board can be used as a prototyping board on an NI ELVIS II Series workstation.

Install and set up the NI Digital Electronics FPGA Board and NI ELVIS II Series workstation as described in the *Where to Start with NI ELVIS II Series* document. Where the NI ELVIS II Series installation instructions refer to the prototyping board, complete the following instructions.

1. Insert the NI Digital Electronics FPGA Board as a prototyping board, as described in the *Where to Start with NI ELVIS II Series* document.
2. Connect one end of the NI Digital Electronics FPGA Board USB cable to the NI Digital Electronics FPGA Board USB connector, and the other end to the USB connector on the host PC.
3. Power on NI ELVIS II Series workstation.
4. Power on the NI Digital Electronics FPGA Board by moving the power switch to the ON position.

   (Windows XP) Windows recognizes any newly installed device the first time the computer reboots after hardware is installed. On some Windows systems, the Found New Hardware Wizard opens with a dialog box for every NI device installed. **Install the software automatically (Recommended)** is selected by default. Click **Next** or **Yes** to install the software for the device and the USB cable ports.

   The green LD-G LED lights, indicating a good connection.

Where to Go From Here

You can now program the FPGA using the onboard USB interface with software, as described in the following chapters:

- Chapter 3, *Programming with LabVIEW Software*

  or

- Chapter 4, *Programming with Xilinx iMPACT Software*

Refer to Chapter 2, *Hardware Components*, for detailed information about the components on the NI Digital Electronics FPGA Board.

Refer to Appendix A, *Specifications*, for device specifications.

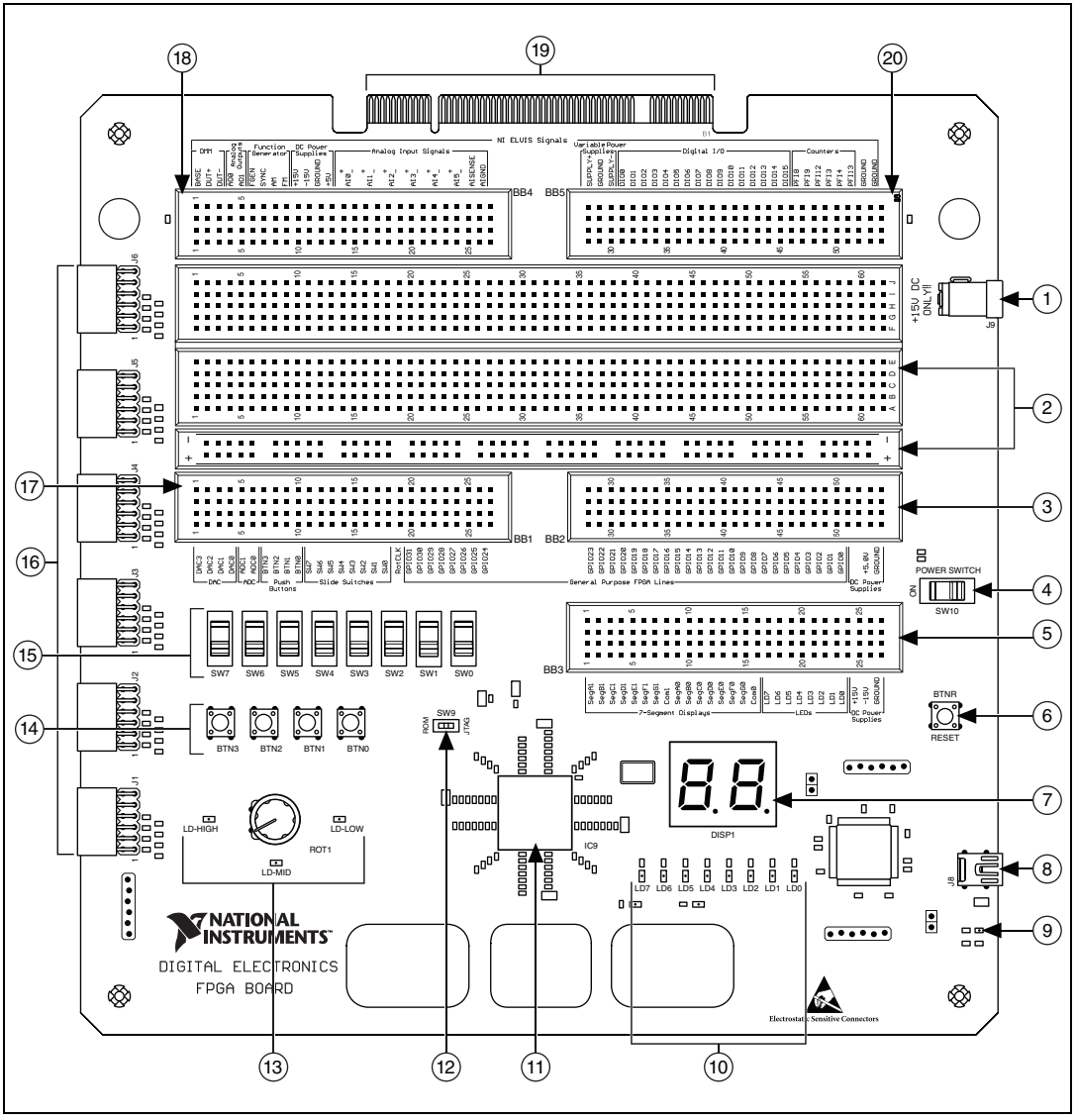
2

Hardware Components

This chapter describes the components on the NI Digital Electronic FPGA Board:

- *Signal Descriptions*
- *Slide Switches*
- *Push Buttons*
- *LEDs*
- *Two Digit Seven-Segment Display*
- *GPIO Lines*
- *Rotary Push-Button Knob and LEDs*
- *50 MHz Onboard Oscillator*
- *FPGA Boot-Up Options*
- *Breadboard Areas*
- *Digilent Pmod Connectors*
- *NI ELVIS Connector*

Figure 2-1 shows a reference diagram of the top view of the NI Digital Electronics FPGA Board.



1 Power Connector	7 Seven-Segment Displays	14 Push Buttons
2 General-Purpose Breadboard Banks	8 USB Connector	15 Slide Switches
3 Signal Breadboard Bank BB2	9 LD-G LED	16 Digilent Pmod Connectors
4 Power Switch	10 LEDs	17 Signal Breadboard Bank BB1
5 Signal Breadboard Bank BB3	11 FPGA	18 Signal Breadboard Bank BB4
6 Reset Button	12 Switch SW9	19 NI ELVIS Connector
	13 Rotary Push-Button Knob/LEDs	20 Signal Breadboard Bank BB5

Figure 2-1. The NI Digital Electronics FPGA Board

Signal Descriptions

Table 2-1 describes the signals found on the NI Digital Electronics FPGA Board signal breadboard banks BB1, BB2, and BB3. Refer to the *Breadboard Areas* section for more information about the breadboards.

Table 2-1. NI Digital Electronics FPGA Board Signals

Signal Name	Reference	Description	Bread-board Bank
DAC<0..3>	GROUND	Digital-to-analog converter signals 0 to 3	BB1
ADC<0..1>	GROUND	Analog-to-digital converter signals 0 to 3	
BTN<0..3>	—	Push Buttons 0 to 3—I/O lines connected to the four push buttons. The push buttons are also connected to the FPGA lines.	
SW<0..7>	—	Slide switches 0 to 7—I/O lines connected to the eight slide switches. The slide switches are also connected to the FPGA lines.	
RotCLK	GROUND	External clock signal—Generates pulses at manually selected frequencies. The external clock output line is *not* connected to the FPGA.	
GPIO<24..31>	GROUND	General-purpose FPGA lines 24 to 31	
GPIO<0..23>	GROUND	General-purpose FPGA lines 0 to 23	BB2
+5.0V	GROUND	DC power supply +5.0 V	
SEGA<0..1>, SEGB<0..1>, SEGC<0..1>, SEGD<0..1>, SEGE<0..1>, SEGF<0..1>, SEGG<0..1>	—	Seven-segment display signals—Controls a specific LED in the seven segments of each digit in the seven-segment display. Segment LEDs are named SEG*x*0 for digit 0, and SEG*x*1 for digit 1. All segment lines are connected to the FPGA.	BB3
COM<0..1>	—	Seven-segment display enable/disable lines—These are enable/disable lines for the corresponding digit (low = enable). Both lines are connected to the FPGA.	
LD<0..7>	—	LEDs 0 through 7—I/O lines connected to the eight LEDs. The LEDs are also connected to the FPGA lines.	
+15V	GROUND	DC power supply +15 V	
–15V	GROUND	DC power supply –15 V	BB3
GROUND	—	DC power supply ground	BB2, BB3

Table 2-2 describes the signals found on signal breadboard banks BB4 and BB5. These signals are only active when the NI Digital Electronics FPGA Board is used in NI ELVIS mode.

Table 2-2. NI ELVIS Mode Signals

Signal Name	Reference	Description	Bread-board Bank
BASE	—	DMM base signal	BB4
DUT+	—	DMM device under test positive line	
DUT–	—	DMM device under test negative line	
AO<0..1>	AIGND	Analog output channels 0 to 1—These terminals supply the voltage output of AO channels 0 to 1.	
FGEN	—	Function generator signal	
SYNC	—	Function generator synchronization signal	
AM	—	Function generator AM signal	
FM	—	Function generator FM signal	
+15V	GROUND	DC power supply +15 V	
–15V	GROUND	DC power supply –15 V	
GROUND	—	DC power supply ground signal	
+5V	GROUND	DC power supply +5 V	
AI<0..5>+	AIGND	Analog input channels 0 to 5 (+)—These pins are routed to the (+) terminal of the respective channel amplifier.	
AI<0..5>–	AIGND	Analog input channels 0 to 5 (–)—These pins are routed to the (–) terminal of the respective channel amplifier.	
AISENSE	—	Analog input sense—In NRSE mode, the reference for each AI <0..5> signal is AI SENSE.	
AIGND	—	Analog input ground—The reference point for analog input and analog output signals.	

Table 2-2. NI ELVIS Mode Signals (Continued)

Signal Name	Reference	Description	Bread-board Bank
SUPPLY+	GROUND	Variable power supply positive line	BB5
GROUND	—	Variable power supply ground	
SUPPLY–	GROUND	Variable power supply negative line	
DIO<0..15>	GROUND	Digital I/O channels 0 to 15—Bidirectional digital I/O channels 0 through 15.	
PFI<3..4>, PFI<8..9>, PFI<12..13>	GROUND	Programmable Function Interface—As an input, each PFI terminal can be used to supply an external source for counter/timer inputs. As a PFI output, you can route the counter/timer outputs to each PFI terminal.	
GROUND	—	Ground—Ground reference for signals.	

Slide Switches

The NI Digital Electronics FPGA Board has eight slide switches, SW0 through SW7, shown in Figure 2-1. Figure 2-2 shows the circuitry of the slide switches.

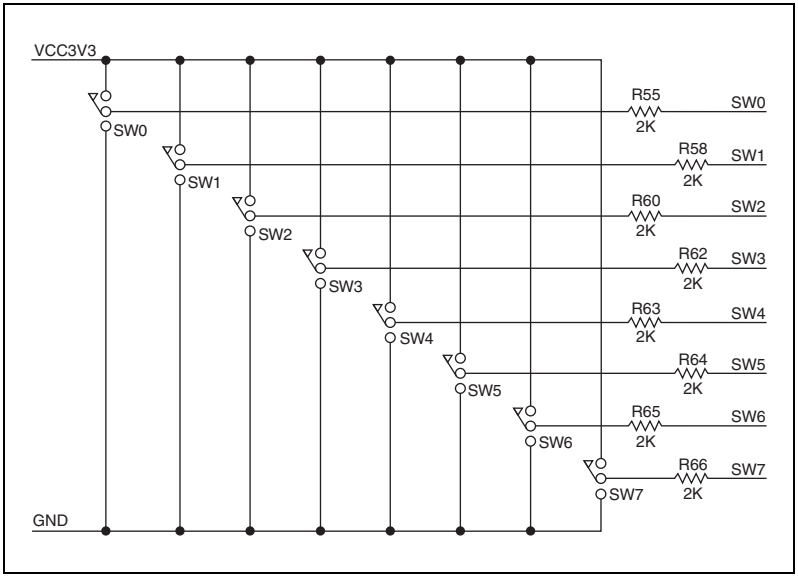


Figure 2-2. Slide Switches Circuit Diagram

The switches typically exhibit about 2 ms of mechanical bounce; there is no active debouncing circuitry. Switches have an output impedance of 2 kΩ. When in the up, or ON, position, the switch connects the line to 3.3 V, a logic High. When in the down, or OFF, position, the switch connects the line to ground, a logic Low.

You can access the slide switch lines through the signal breadboard, BB1. For more information about the signal breadboards, refer to the *Signal Breadboard Area* section. The switches are also connected directly to the FPGA lines. Refer to the *UCF File Constraints* section of Chapter 4, *Programming with Xilinx iMPACT Software*, for more information about accessing the FPGA signals in iMPACT.

Push Buttons

The NI Digital Electronics FPGA Board has four momentary-contact push-buttons, BTN0 through BTN3, shown in Figure 2-1. Figure 2-3 shows the circuitry of the push buttons.

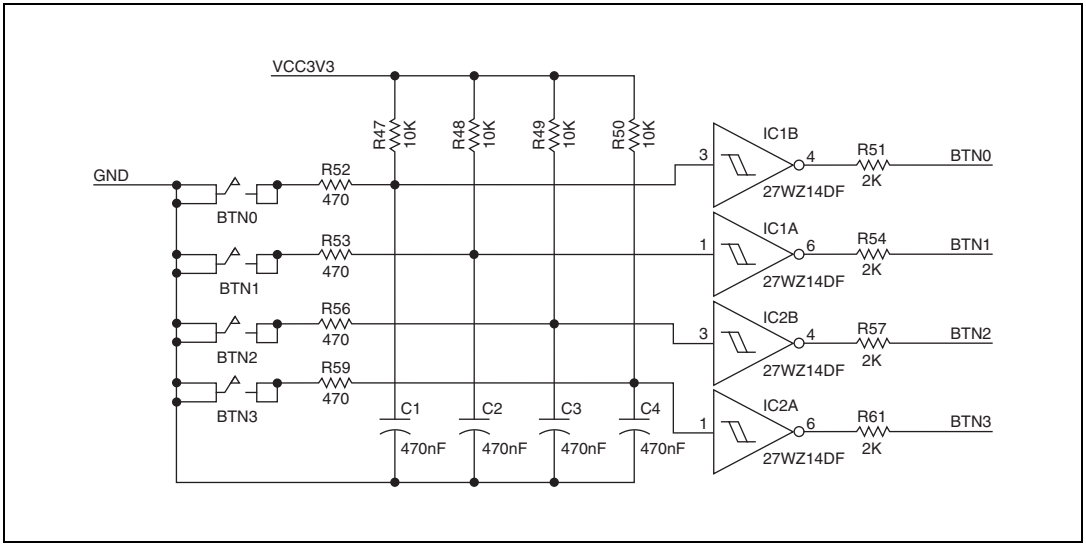


Figure 2-3. Push Buttons Circuit Diagram

Pressing a push button connects a logic Low into an inverter, which outputs a logic High of 3.3 V into the associated line, as shown in Figure 2-3. When the push button is not pressed, the power line goes into the inverter, which outputs a logic Low into the associated line. Debouncing circuitry is implemented using a resistor and a capacitor on the push button signal line.

You can access the push button lines through the signal breadboard, BB1. For more information about the signal breadboards, refer to the *Signal Breadboard Area* section. The buttons are also connected directly to the FPGA lines. Refer to the *UCF File Constraints* section of Chapter 4, *Programming with Xilinx iMPACT Software*, for more information about accessing the FPGA signals in iMPACT.

LEDs

The NI Digital Electronics FPGA Board has eight individual surface-mount LEDs, LD0 through LD7, shown in Figure 2-1. Figure 2-4 shows the circuitry of the LEDs.

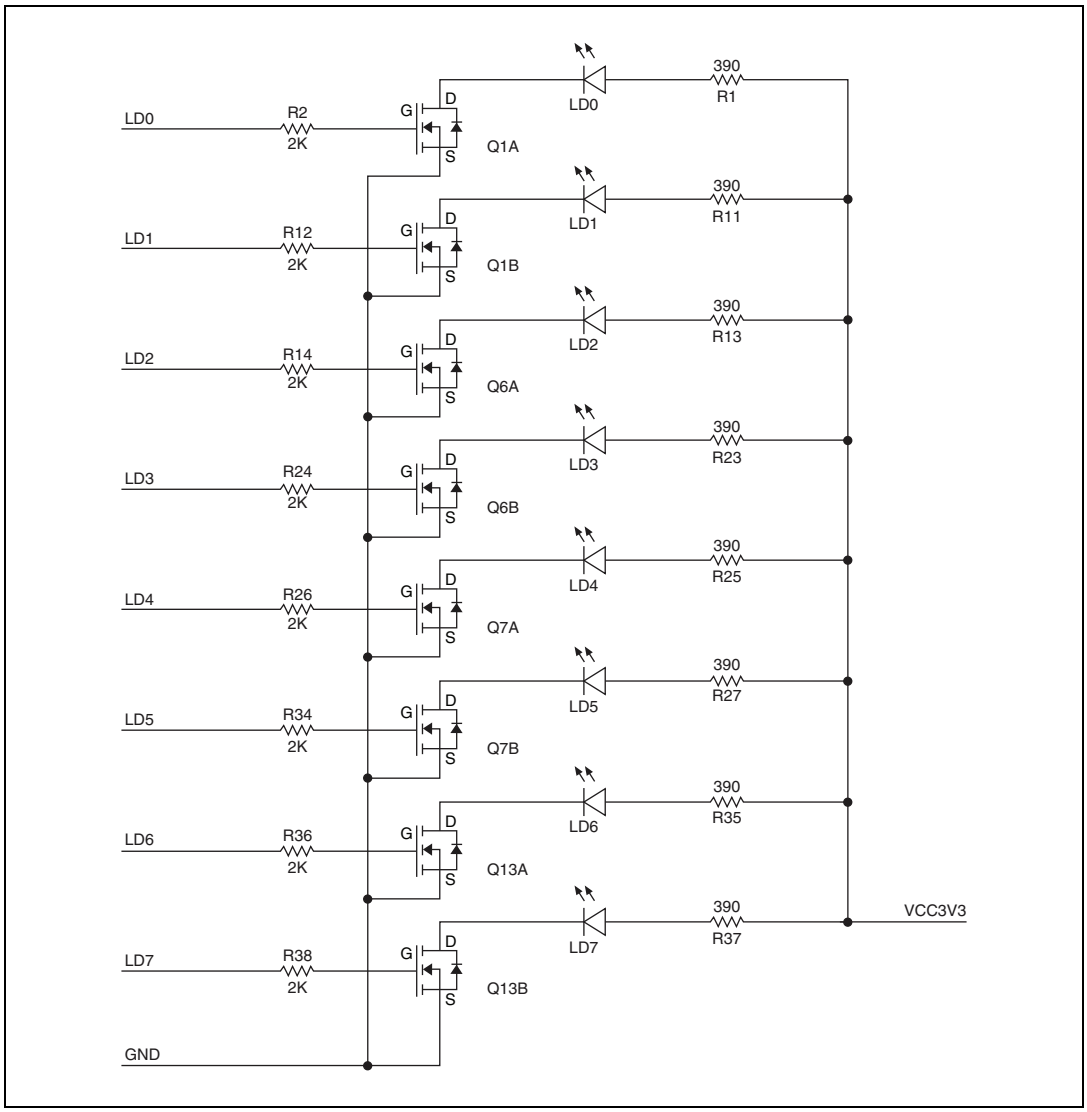


Figure 2-4. LEDs Circuit Diagram

Each LED is connected on one side through a 390 Ω current-limiting resistor to the power line, and connected on the other side through a CMOS driver, as shown in Figure 2-4.

You can access the LED lines through the signal breadboard, BB3. To light an individual LED, drive the associated line High (3.3 V or 5 V). For more information about the signal breadboards, refer to the *Signal Breadboard*

Area section. The LEDs are also connected directly to the FPGA lines. To light an individual LED, drive the associated FPGA control signal High. Refer to the *UCF File Constraints* section of Chapter 4, *Programming with Xilinx iMPACT Software*, for more information about accessing the FPGA signals in iMPACT.

Two Digit Seven-Segment Display

The NI Digital Electronics FPGA Board has a two digit seven-segment display, DISP1, in a common cathode configuration. Refer to Figure 2-1 for the location of the two seven-segment display. The two digit seven-segment display circuitry is shown in Figure 2-5.

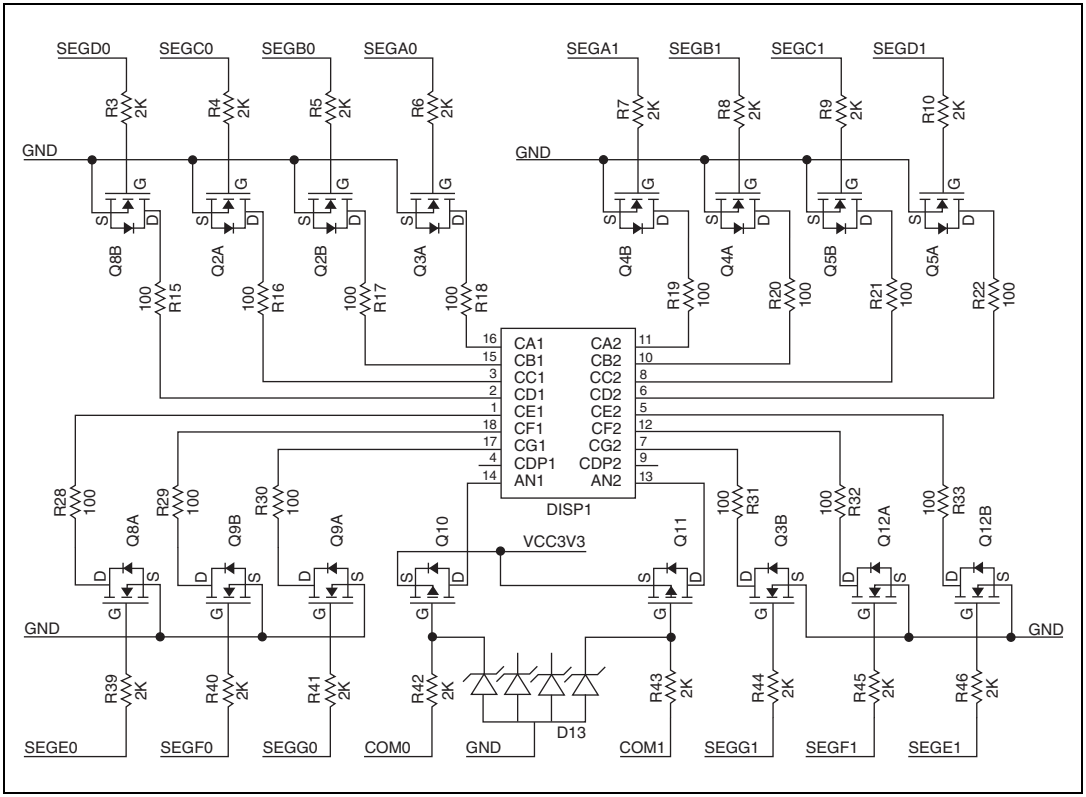


Figure 2-5. Two Digit Seven-Segment Display Circuit Diagram

Each digit is composed of seven segments arranged in a figure 8 pattern, with an LED embedded in each segment. Segment LEDs are SEG*x*0 for digit 0, and SEG*x*1 for digit 1, as shown in Figure 2-6.

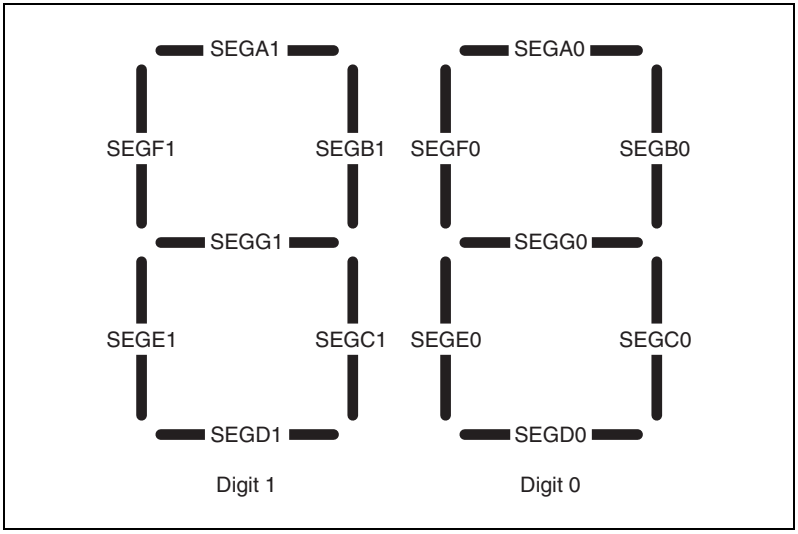


Figure 2-6. Segment Diagram

Segment LEDs can be individually illuminated, so different patterns can be displayed on a digit by lighting certain LED segments. You can access the seven-segment display lines through the signal breadboard, BB3. To light an individual LED segment, drive the associated line High (using 3.3 V or 5 V). Lines COM0 and COM1 can be used to enable/disable each digit of the display to allow using the display in multiplexed mode. For more information about the signal breadboards, refer to the *Signal Breadboard Area* section.

All segment and COM lines are connected to the FPGA. Refer to the *UCF File Constraints* section of Chapter 4, *Programming with Xilinx iMPACT Software*, for more information about accessing the FPGA signals in iMPACT.

GPIO Lines

The NI Digital Electronics FPGA Board has 32 general-purpose I/O lines, GPIO0 to GPIO31. Figure 2-7. shows the circuitry of the GPIO lines.

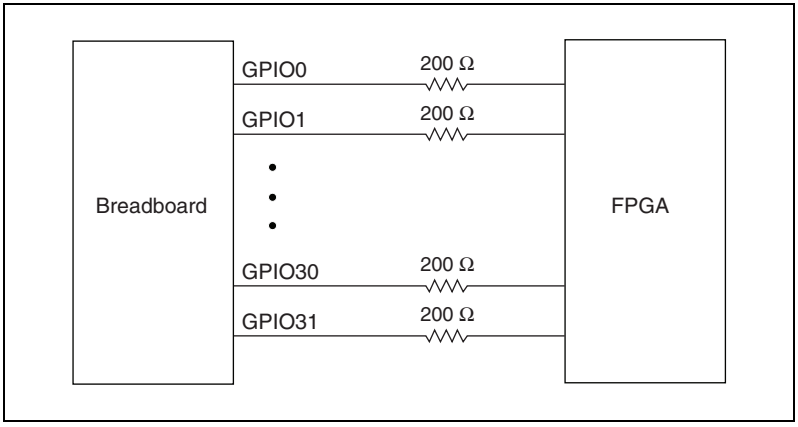


Figure 2-7. GPIO Lines Circuit Diagram

Each GPIO line is connected to the FPGA through a 200 Ω current-limiting resistor. You can access the GPIO lines through signal breadboards BB1 and BB2. For more information about the signal breadboards, refer to the *Signal Breadboard Area* section.

GPIO lines can be configured in software on a per-line basis for input or output. GPIO lines are 3.3 V CMOS type and +5 V tolerant.

Rotary Push-Button Knob and LEDs

The NI Digital Electronics FPGA Board has a rotary push-button knob, ROT1, that is used to set the frequency range and value inside the range for an external clock generated by a microcontroller.

Pressing the rotary push-button knob selects the range, which is indicated by frequency range LEDs. The rotary push-button knob and frequency range LEDs are shown in Figure 2-1. The frequency range LEDs have the following functionality:

- **LD-LOW**—When lit, the external clock generates a 1 Hz to 100 Hz clock frequency that is controlled by rotating the knob.
- **LD-MID**—When lit, the external clock generates a 100 Hz to 100 kHz clock frequency that is controlled by rotating the knob.

- **LD-HIGH**—When lit, the external clock generates a 100 kHz to 5 MHz clock frequency that is controlled by rotating the knob.

You can access the external clock output line using signal line RotClk, located on breadboard BB1. For more information about the signal breadboards, refer to the *Signal Breadboard Area* section.

The external clock output line is *not* connected to the FPGA.

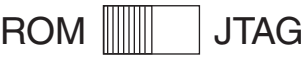
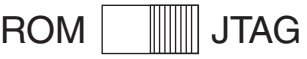
50 MHz Onboard Oscillator

The NI Digital Electronics FPGA Board uses a 50 MHz onboard clock oscillator as the clock input. The 50 MHz clock output line, GCLK0, is connected to FPGA line B8. Refer to the *UCF File Constraints* section of Chapter 4, *Programming with Xilinx iMPACT Software*, for more information about accessing the FPGA signals in iMPACT.

FPGA Boot-Up Options

Boot-up selection on the NI Digital Electronics FPGA Board is controlled by switch SW9, shown in Figure 2-1. The two FPGA boot-up options are described in Table 2-3.

Table 2-3. FPGA Boot-Up Options

FPGA Boot-Up Option	Switch Position
Boot-up from ROM (default)—Configures the FPGA from the image stored in the Platform Flash PROM.	
Boot-up from JTAG—Does not load anything into the FPGA, waits for program download from USB-JTAG port.	

The NI Digital Electronics FPGA Board supports download of FPGA designs directly to the FPGA through the JTAG, using the onboard USB interface. Switch SW9 should be set in the default position ROM. The board boots up in default configuration, which can be overwritten by the downloaded FPGA design. The downloaded FPGA design is valid as long as the board is not powered down, reset, or rewritten with a different FPGA design.

Breadboard Areas

The NI Digital Electronics FPGA Board features two breadboard areas:

- *Signal Breadboard Area*
- *General-Purpose Breadboard Area*

Refer to Figure 2-1 for the location of the breadboard areas.

Signal Breadboard Area

The signal breadboard area is comprised of breadboard banks BB1, BB2, BB3, BB4, and BB5. Refer to Figure 2-1 for the locations of the signal breadboard banks. Refer to Tables 2-1 and 2-2 for descriptions of signals found on the signal breadboard area.

- **BB1**—Breadboard area for the DAC, ADC, push buttons, slide switches, external clock, and general-purpose FPGA lines.
- **BB2**—Breadboard area for the general-purpose FPGA lines and DC power supplies.
- **BB3**—Breadboard area for the seven-segment displays, LEDs, and DC power supplies.
- **BB4**—Breadboard area for the NI ELVIS signals, including analog input, analog output signals, function generator, DC power supplies, and digital input/output signals.
- **BB5**—Breadboard area for the NI ELVIS signals, including the variable power supplies, digital I/O signals, counter signals, and ground references.

General-Purpose Breadboard Area

The general-purpose breadboard area contains two breadboard banks. These banks are not connected to any board resources. Refer to Figure 2-1 for the locations of the general-purpose breadboard banks.

Note Signal breadboard banks BB4 and BB5 can be used as general-purpose breadboards when the NI Digital Electronics FPGA Board is used in stand-alone mode.

Digilent Pmod Connectors

Use the Digilent Pmod connectors, shown in Figure 2-1, for connection to up to six Digilent Pmod modules. Digilent Pmods are compact modules that can be added to expand the capabilities of the NI Digital Electronics FPGA Board.

You can connect up to six 1×6 single or 2×6 double Pmod modules to the NI Digital Electronics FPGA Board. Refer to the Digilent Web site, `www.digilentinc.com`, for more information about Pmod modules.

NI ELVIS Connector

The NI Digital Electronics FPGA Board features a PCI type connector, shown in Figure 2-1, which plugs into an NI ELVIS II Series workstation when the NI Digital Electronics FPGA Board is used in NI ELVIS mode.

3

Programming with LabVIEW Software

After you install the software and set up the hardware for stand-alone mode or NI ELVIS mode as described in Chapter 1, *Overview and Setup*, you are ready to program with NI LabVIEW software and the LabVIEW FPGA Module.

This chapter lists information necessary to program the NI Digital Electronics FPGA Board with LabVIEW and the LabVIEW FPGA Module, including a tutorial section that demonstrates how to create and run your own LabVIEW project.

Building a LabVIEW FGPA Design

This section demonstrates how to create a LabVIEW project and FPGA VI that performs the following:

- Routes switch SW0 to LED0, which causes LED0 to light when switch SW0 is moved to the ON position, and turn off when the switch moved to the OFF position.
- Routes push button BTN0 to LED2, which causes LED2 to light when button BTN0 is pressed, and turn off when the button is depressed.

This example also demonstrates how to compile and run the FPGA VI on the NI Digital Electronics FPGA Board.

To begin programming with LabVIEW, connect the USB cable to the NI Digital Electronics FPGA Board, apply power to the board, and move the power switch to the ON position.

Creating a Project

1. Launch LabVIEW.
2. In the **Getting Started** window, click **Empty Project**. The new project opens in the **Project Explorer** window.
3. Save the project as `FPGA_Design.lvproj`.

Creating an FPGA Target VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»Targets and Devices**.
2. In the **Add Targets and Devices on My Computer** window, select **New target or device**, expand **ELVIS**, and highlight **DE FPGA Board**. Click **OK**. The target is discovered and the target and target properties are loaded into the project tree.
3. In the **Project Explorer** window, right-click **FPGA Target (Board1, DE FPGA Board)** and select **New»FPGA I/O**. The **New FPGA I/O** window opens.
4. In the Available Resources pane, expand **Slide Switches** and select **SW0**. Click **Add** to move SW0 to the New FPGA I/O pane. This adds this FPGA resource to the project.
5. Expand **Push Buttons** and select **BTN0**. Click **Add** to move BTN0 to the New FPGA I/O pane.
6. Expand **LEDs** and select **LED0** and **LED2**. Click **Add** to move the LEDs to the New FPGA I/O pane.
7. Click **OK**. Notice that the selected FPGA resources were added to the FPGA Target tree in the **Project Explorer** window, as shown in Figure 3-1.

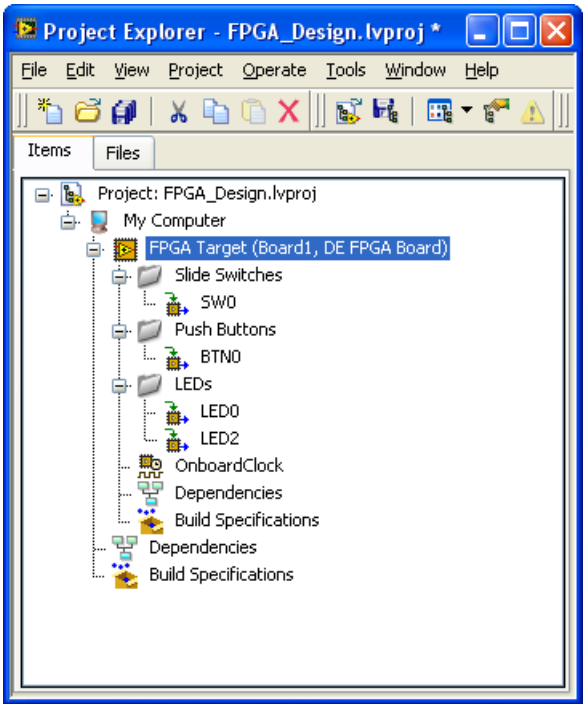


Figure 3-1. FPGA Target Tree with New FPGA Resources

8. In the **Project Explorer** window, right-click **FPGA Target (Board1, DE FPGA Board)**, and select **New»VI**. A blank VI opens. Select the block diagram window.
9. In the **Project Explorer** window FPGA Target (Board1, DE FPGA Board) tree view, select **SW0** and **LED0** and drag them onto the block diagram as shown in Figure 3-2.
10. In the LabVIEW block diagram, wire SW0 output to the LED0 input.
11. In the Project Explorer window FPGA Target (Board1, DE FPGA Board) tree view, select **BTN0** and **LED2** and drag them onto the block diagram.
12. In the LabVIEW block diagram, wire BTN0 output to the LED2 input.
13. Add a While Loop around the resources.

14. Wire a false constant to the stop condition of the While Loop.

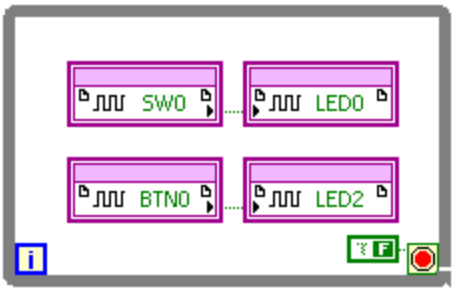


Figure 3-2. Block Diagram

Tip Click the **Clean Up Diagram** button on the toolbar to tidy VI block diagrams.

15. Save the VI as `FPGA_Design.vi`.

Running the FPGA VI

1. Verify that the USB cable is connected to the NI Digital Electronics FPGA Board and host PC, and the power switch is moved to the ON position.
2. Open the front panel of `FPGA_Design.vi`.
3. Click the **Run** button to run the VI.

   The application compiles VHDL code and generates a bitstream file that is downloaded into the FPGA configuration storage.

   The **Generating Intermediate Files** window opens and displays the compilation progress. The **LabVIEW FPGA Compile Server** window opens and runs. The compilation takes several minutes.
4. When the compilation finishes, click the **Stop Server** button to close the LabVIEW FPGA Compile Server.
5. Click **OK** in the **Successful Compile Report** window.

   The application is running on the FPGA board at this time.
6. Move switch SW0 up and down; LED0 should correspondingly light and turn off.
7. Press button BTN0; LED2 should correspondingly light and turn off.

More LabVIEW Example Programs

You can find additional LabVIEW example programs in the LabVIEW examples folder that installed with the NI Digital Electronics FPGA Board software driver by navigating to `LabVIEW 8.6\examples\DE FPGA Board`. For detailed information about LabVIEW examples for the NI Digital Electronics FPGA Board, refer to the Developer Zone document, *NI Digital Electronics FPGA Board – LabVIEW Example Programs*. To access this document, go to `ni.com/info` and enter the info code `defblv`.

LabVIEW FPGA and CLIP

The Component-Level Intellectual Property (CLIP) node is a framework for importing external field-programmable gate array intellectual property (FPGA IP) into the NI LabVIEW FPGA Module.

There are two types of CLIP:

- User-defined CLIP allows users to insert VHDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI. The NI Digital Electronics FPGA Board supports user-defined CLIP.
- Socketed CLIP, provides the same IP integration functionality of the user-defined CLIP, while also allowing the CLIP to communicate directly with circuitry external to the FPGA. Socketed CLIP is *not* supported in the NI Digital Electronics FPGA Board.

The CLIP feature targets users with digital design experience, a general knowledge of VHDL, and a working understanding of XML. For the more information, refer to the *Using VHDL Code as Component-Level IP* topic in the *FPGA Module* book of the *LabVIEW Help*.

Adding User-Defined CLIP to an FPGA Target

Refer to the *Using VHDL Code as Component-Level IP* topic in the *FPGA Module* book of the *LabVIEW Help* for additional information about using CLIP with the NI Digital Electronics FPGA Board. For detailed information about the NI Digital Electronics FPGA Board and CLIP, including software tutorials, refer to the Developer Zone document, *Importing External IP into LabVIEW FPGA with the CLIP Node*. To access this document, go to `ni.com/info` and enter the info code `clipdz`.

Running a VI in Emulation Mode

You can run a VI written for the NI Digital Electronics FPGA Board in emulation mode. Emulation mode, when the computer executes code written for another target (FPGA in this case), is useful in the debugging and testing phase of an FPGA application because it reduces the need for repetitive VI compilation during development.

Compiling an FPGA VI can take minutes to hours. You can test the logic of an FPGA VI written for the NI Digital Electronics FPGA Board before compilation by running the FPGA VI on a development computer with simulated I/O. When you run an FPGA VI on a development computer with simulated I/O, LabVIEW generates random data for the inputs or uses a custom VI that you create to simulate I/O. You can use all traditional LabVIEW debugging techniques, such as probes, execution highlighting, breakpoints, and single-stepping. You cannot test certain aspects of VI behavior, such as timing and determinism.

For detailed information about running an NI Digital Electronics FPGA Board VI in emulation mode, including software examples, refer to the Developer Zone document, *Running a Digital Electronics FPGA Board VI in Emulation Mode on a Development Computer*. To access this document, go to `ni.com/info` and enter the info code `defbem`.

Programming the PROM

To change the default FPGA power-up application, you must download the LabVIEW FPGA VI to the FPGA flash PROM by completing the following steps.

1. In the Project Explorer, right-click the target VI and select **Download VI to Flash Memory**.
2. LabVIEW displays the programming process. When the LabVIEW FPGA window displays **`Download successful`**, click **OK**.

You can return to the default power-up configuration by using the Flash_Image example, located in the `LabVIEW 8.6\examples\DE FPGA Board` folder.

Testing the Download

To test that the download was successful, complete the following steps.

1. Verify that switch SW9 is in the ROM position.

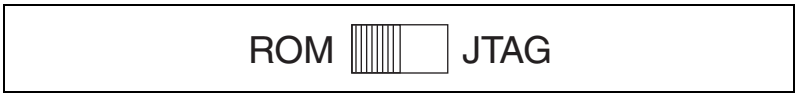


Figure 3-3. Switch SW9 in ROM Position

2. Reboot the NI Digital Electronics FPGA Board by pressing the reset button.
3. Verify that the FPGA is running the (PROM) downloaded application.

Where to Go from Here

The following resources contain information about writing applications for the NI Digital Electronics FPGA Board:

- LabVIEW FPGA documentation:
  - *Getting Started with LabVIEW FPGA 8.x*—This KnowledgeBase, available at `ni.com/kb`, provides links to the top resources that can be used to assist in getting started with programming in LabVIEW FPGA.
  - *FPGA Module* book in the *LabVIEW Help*—Select **Help»Search the LabVIEW Help** in LabVIEW to view the *LabVIEW Help*. Browse the **FPGA Module** book in the **Contents** tab for information about how to use the FPGA Module to create VIs that run on the NI Digital Electronics FPGA Board.
  - *LabVIEW FPGA Module Release and Upgrade Notes*—Contains information about installing the LabVIEW FPGA Module, describes new features, and provides upgrade information. To access this document, refer to `ni.com/manuals`. In LabVIEW 8.0 or later, you can also view the LabVIEW Manuals directory that contains this document by selecting **Start»All Programs»National Instruments»LabVIEW»LabVIEW Manuals**.
- *LabVIEW FPGA IPNet*—Offers resources for browsing, understanding, and downloading LabVIEW FPGA functions or IP (Intellectual Property). Use this resource to acquire IP that you need for your application, download examples to help learn programming techniques, and explore the depth of IP offered by the LabVIEW FPGA platform. To access the LabVIEW FPGA IPNet, visit `ni.com/ipnet`.

4

Programming with Xilinx iMPACT Software

After you install the software and set up the hardware for stand-alone mode as described in Chapter 1, *Overview and Setup*, you are ready to program with Xilinx iMPACT software.

This chapter lists information necessary to program the NI Digital Electronics FPGA Board with Xilinx iMPACT.

Xilinx iMPACT Software Examples

For detailed information about Xilinx iMPACT software examples for the NI Digital Electronics FPGA Board, refer to the Developer Zone document, *Xilinx iMPACT Examples*. To access this document, go to `ni.com/info` and enter the info code `impactex`. You can also refer to the Xilinx University Program Web site at `www.xilinx.com/univ/`.

UCF File Constraints

This section lists the UCF file (`.ucf`) constraints for the various hardware components of the NI Digital Electronics FPGA Board. Refer to Chapter 2, *Hardware Components*, for more information about the hardware components listed here.

Slide Switches

The UCF file constraints for the eight slide switches, SW0 to SW7, are listed as follows. SW*x* refers to the slide switch line, LOC indicates the FPGA line location, and IOSTANDARD is the I/O standard used.

```
Net "SW0" LOC="J11" | IOSTANDARD = LVCMOS33;
Net "SW1" LOC="J12" | IOSTANDARD = LVCMOS33;
Net "SW2" LOC="H16" | IOSTANDARD = LVCMOS33;
Net "SW3" LOC="H13" | IOSTANDARD = LVCMOS33;
Net "SW4" LOC="G12" | IOSTANDARD = LVCMOS33;
Net "SW5" LOC="E14" | IOSTANDARD = LVCMOS33;
Net "SW6" LOC="D16" | IOSTANDARD = LVCMOS33;
Net "SW7" LOC="B16" | IOSTANDARD = LVCMOS33;
```

Push Buttons

The UCF file constraints for the four push buttons, BTN0 to BTN3, are listed as follows. BTN*x* refers to the push button line, LOC indicates the FPGA line location, and IOSTANDARD is the I/O standard used.

```
Net "BTN0" LOC="C13" | IOSTANDARD = LVCMOS33;
Net "BTN1" LOC="D12" | IOSTANDARD = LVCMOS33;
Net "BTN2" LOC="C12" | IOSTANDARD = LVCMOS33;
Net "BTN3" LOC="C10" | IOSTANDARD = LVCMOS33;
```

LEDs

The UCF file constraints for the eight LEDs, LED0 to LED7, are listed as follows. LED*x* refers to the LED line, LOC indicates the FPGA line location, IOSTANDARD is the I/O standard used, SLEW refers to the slew rate, the maximum rate of change of a signal, and DRIVE indicates the current drive strength on the FPGA in milliamps.

```
Net "LED0" LOC="C11" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "LED1" LOC="D11" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "LED2" LOC="B11" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "LED3" LOC="A12" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "LED4" LOC="A13" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "LED5" LOC="B13" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "LED6" LOC="A14" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "LED7" LOC="B14" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
```

Seven-Segment Displays

The UCF file constraints for the seven-segment displays are listed as follows: SEG*xx* refers to the display segment line, COM*x* refers to the display anode line, LOC indicates the FPGA line location, IOSTANDARD is the I/O standard used, SLEW refers to the slew rate, the maximum rate of change of a signal, and DRIVE indicates the current drive strength on the FPGA in milliamps.

```
Net "SEGA0" LOC="E3" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGB0" LOC="E1" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGC0" LOC="G5" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGD0" LOC="D1" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGE0" LOC="E4" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGF0" LOC="C1" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGG0" LOC="C2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "COM0" LOC="B2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
```

```
Net "SEGA1" LOC="H6" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGB1" LOC="K2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGC1" LOC="H3" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGD1" LOC="K1" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGE1" LOC="G4" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGF1" LOC="J2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "SEGG1" LOC="G3" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
Net "COM1" LOC="G2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8;
```

50 MHz Clock Input Source

The UCF file constraints for the 50 MHz clock input source are listed as follows.

```
Net "sys_clk_pin" LOC="B8";

Net "sys_clk_pin" IOSTANDARD = LVCMOS33;

## System level constraints
Net "sys_clk_pin" TNM_NET = sys_clk_pin;
TIMESPEC TS_sys_clk_pin = PERIOD "sys_clk_pin" 20000 ps;
```

Programming the PROM

To program the formatted PROM file into the platform flash PROM through the onboard USB JTAG circuitry, connect the USB cable to the NI Digital Electronics FPGA Board, apply power to the board, move the power switch to the ON position, and complete the following steps.

1. On the NI Digital Electronics FPGA Board, move switch SW9 to the JTAG position.

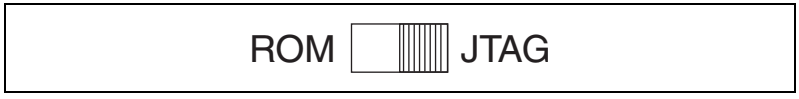


Figure 4-1. Switch SW9 in JTAG Position

2. Launch Xilinx ISE.
3. Select **File»Open Project**, and navigate to the location of `PROM.ise`. Click **OK**.
4. In the Processes pane of the project window, expand **Configure Target Device**.
5. Double-click **Manage Configuration Project (iMPACT)**. The Transcript pane of the project window displays the configuration progress.

The iMPACT - Welcome to iMPACT window opens.

Note If the iMPACT - Welcome to iMPACT window does not open, launch iMPACT by selecting **Start»Programs»Xilinx ISE Design Suite»ISE»Accessories»iMPACT**.

6. Select **Configure devices using Boundary-Scan (JTAG)** and **Automatically connect to a cable and identify Boundary-Scan chain** (these should be selected by default). Click **Finish**.

   The Assign New Configuration File window opens.

7. Select the `main.bit` configuration file in the Assign New Configuration File window. Click **Open**.

   You have the option of selecting additional configuration files. Because you do not need a new configuration, click **Cancel**.

   The Device Programming Properties window opens.

8. In the Device Programming Properties window, select **Device 1 (FPGA, xc3s500e)** to program Device 1. The NI Digital Electronics FPGA Board FPGA is a Xilinx XC3S500E Spartan-3E FPGA.
9. Click **OK**. The Boundary Scan pane opens in the project window.
10. Right-click the **xcf04s file ?** icon, and select **Assign New Configuration File** to assign the PROM file (`.mcs`), to the XCF04S platform flash PROM on the JTAG chain.

    Click **Open**.

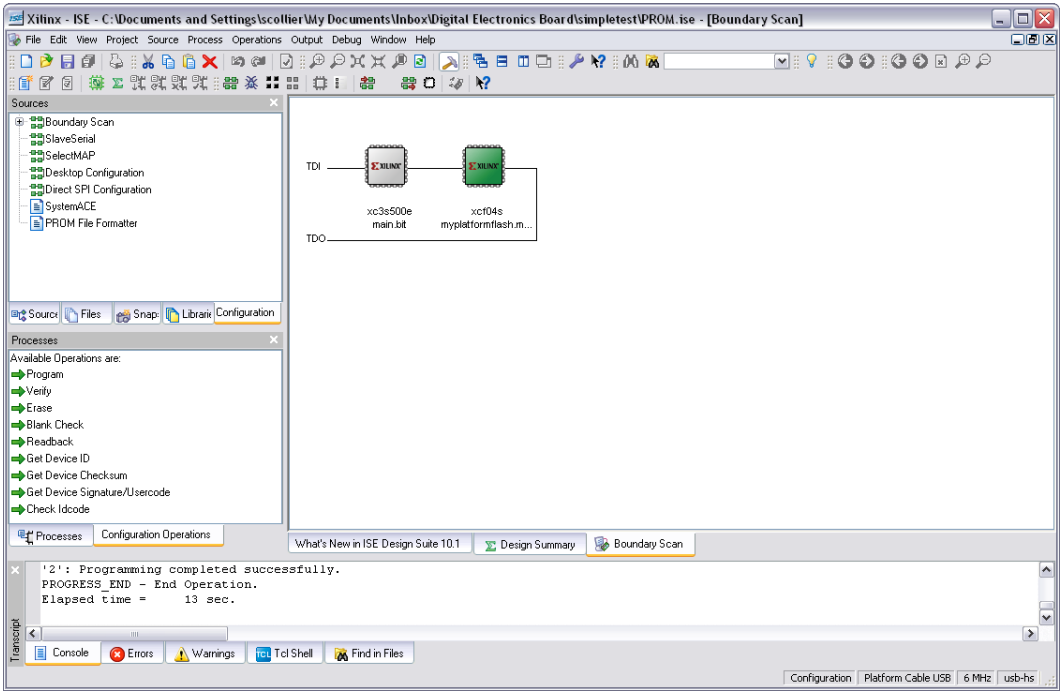


Figure 4-2. PROM.ise Project Window (Boundary Scan)

11. Right-click the **xcf04s myplatformflash.mcs** icon and select **Program**.
12. In the Device Programming Properties window, select **Device 2 (PROM, xcf04s)**, the PROM type to be programmed.
13. Put a check mark in the following Device Programming Properties options:
    - **Verify**—Verifies the PROM is correctly programmed and matches the downloaded configuration bitstream. This option is recommended though it increases overall programming time.
    - **Erase Before Programming**—Erases the platform flash PROM completely before programming, ensuring that no previous data lingers. This option is recommended though it increases overall programming time.
    - **Load FPGA**—Forces the FPGA to reconfigure after programming the platform flash PROM.

Click **OK**. A Progress Dialog window opens and displays the execution progress.

After the PROM is successfully programmed, the Boundary Scan pane displays **`Program Succeeded`**.

14. Select **File»Close Project** and save all changes.

Testing the Download

To test that the download was successful, complete the following steps.

1. Verify that switch SW9 is in the ROM position.

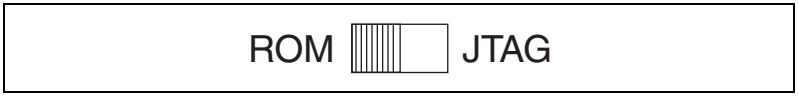


Figure 4-3. Switch SW9 in ROM Position

2. Reboot the NI Digital Electronics FPGA Board by pressing the reset button.
3. Verify that the FPGA is running the (PROM) downloaded application.

Where to Go from Here

The following resources contain information for writing applications and taking measurements with the NI Digital Electronics FPGA Board:

- *ISE Quick Start Tutorial*—Contains a step-by-step description of creating a simple design, performing simulation, and running implementation.
- *Xilinx ISE Help*—Describes how to get started with the ISE Design Suite software, FPGA design, and troubleshoot the software.

A

Specifications

Specifications listed below are typical at 25 °C unless otherwise noted.

FPGA

FPGA ..... Xilinx XC3S500E-4FTG256C
- System gates ..... 500 k
- Logic cells 10,476
- Logic family ..... CMOS

Platform Flash configuration PROM ..... 4 Mbit

Onboard USB-based FPGA/CPLD download/debug interface

General-Purpose I/O

GPIO lines ..... 32 general-purpose digital I/O lines, 3.3 V, 8 mA maximum

Analog Output

Channels 4

Resolution ..... 12 bits

Range
- DAC0, DAC1 ..... 0–3.3 V
- DAC2, DAC3 ..... 0–2.5 V

Generation ..... Single point

Analog Input

Channels 2

Resolution.....12 bits, simultaneously sampled

Range .....0–3.3 V

Sample-and-hold acquisition time .....39 ns

Acquisition.....Single point

General

ON/OFF power switch.....1

Reset Button 1

LEDs (discrete).....8

Slide switches 8

Push buttons.....4

Seven-segment displays.....2

Rotary encoder with
push-button shaft 1

Clock oscillator.....50 MHz clock oscillator

12-pin expansion connectors (Pmod) .....6, Digilent

Signal breadboard area

- For NI ELVIS 2
- For FPGA 3

General-purpose breadboard area.....1

NI ELVIS connector interface.....1, PCI type

Bus Interface

USB .....USB 2.0 Full-Speed

USB connector.....Mini-USB Type B

Power

DC power supply ..... 15 VDC, 650 mA

Power supplies

+15 V ..... 1.5 A maximum[1]

–15 V..... 150 mA maximum[1]

+5 V ..... 400 mA maximum[1]

Total combined power ..... 6 W maximum[1]

Physical

Dimensions..... 20.9 cm × 21.6 cm (8.25 in. × 8.5 in.)

Weight..... 284 g (10 oz)

Maximum Working Voltage

Breadboard areas are only intended to be used for low voltage circuits (<42 VAC, 60 VDC).

Environmental

Operating temperature..... 0 to 50 °C

Storage temperature ..... 0 to 50 °C

Relative humidity..... 5 to 85% RH, noncondensing

Pollution Degree (indoor use only)..... 2

Maximum altitude..... 2,000 meters

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

[1] Total combined power of 6 W is available in an idle state. Available power will decrease with increased FPGA utilization.

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

Note For EMC compliance, operate this product according to the documentation.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

National Instruments is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of their life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit `ni.com/environment/weee.htm`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。
关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。
(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

B

Technical Support and Professional Services

Visit the following sections of the award-winning National Instruments Web site at ni.com for technical support and professional services:

- **Support**—Technical support at ni.com/support includes the following resources:
  - **Self-Help Technical Resources**—For answers and solutions, visit ni.com/support for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at ni.com/forums. NI Applications Engineers make sure every question submitted online receives an answer.
  - **Standard Service Program Membership**—This program entitles members to direct access to NI Applications Engineers via phone and email for one-to-one technical support as well as exclusive access to on demand training modules via the Services Resource Center. NI offers complementary membership for a full year after purchase, after which you may renew to continue your benefits.

    For information about other technical support options in your area, visit ni.com/services, or contact your local office at ni.com/contact.
- **Training and Certification**—Visit ni.com/training for self-paced training, eLearning virtual classrooms, interactive CDs, and Certification program information. You also can register for instructor-led, hands-on courses at locations around the world.
- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.

- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting `ni.com/certification`.

If you searched `ni.com` and could not find the answers you need, contact your local office or NI corporate headquarters. Phone numbers for our worldwide offices are listed at the front of this manual. You also can visit the Worldwide Offices section of `ni.com/niglobal` to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

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